

RC7321

Three-State ATE Pin Electronics Driver

Features

- High output slew rate (1.3 V/ns typical)
- Wide output voltage range (-2.2V to +7V), and up to 9.2 Vp-p swings
- Three-state/high impedance output
- High repetition rate (250 MHz for ECL swings)
- Low output offset (40 mV typical) and output offset drift (0.1 mV/°C typical).
- Low leakage (10 nA typical) and low output capacitance (3 pF typical) in high impedance inhibit mode
- High speed differential inputs with wide common mode range for ease of interface to ECL as well as TTL and CMOS levels
- Output short circuit protection (Safe Operating Area protection with current limiting and thermal shutdown)
- 100 mA typical dynamic current drive capability
- Absolute slew rate control
- Available in 28-pin PLCC

Applications

- ATE pin electronics driver
- Precision waveform generator
- Level translator
- PCB & Burn-in ATE Driver
- General purpose driver for PCB & burn-in test systems
- Laser driver
- CRT preamplifier

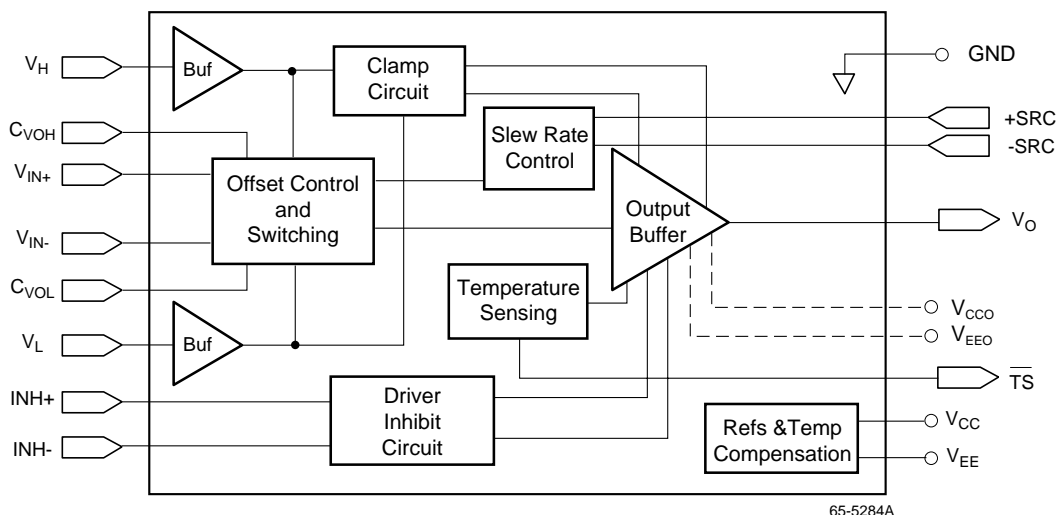
Description

The RC7321 is a low cost Pin Electronics Driver designed for use in all high speed ATE systems which require pin drivers with three state capability and high slew rates. The RC7321 has the ability to drive a 50Ω transmission line of up to 2 feet in length with a slew rate of 1.2 V/ns and repetition rate of over 250 MHz for ECL output levels. These features, combined with a maximum output swing of 9.5 Vp-p over the range of -2.5V to +7V, provide this circuit with the ability to test TTL, CMOS, ECL and GaAs devices. The high and low limits of the output swing are set through the program pins V_H and V_L, respectively. The transfer characteristic from the program pins to the output pin is unity gain with very low offset drift. The V_H and V_L inputs have been buffered to operate with low bias currents (1 μA typical) allowing direct coupling to the output of a DAC.

When the RC7321 is used on an I/O pin, it may be forced into the high impedance state through the INH+ and INH- differential inputs. In the high impedance state, excellent isolation is provided between the output of the disabled driver and the pin by virtue of low driver output capacitance (3.0 pF typical) and low output leakage (10 nA typical).

The RC7321 is provided with high speed differential ECL inputs for ease of interface with the differential ECL outputs of a timing generator. The inputs have a voltage range of -2V to +6V, so that if required, an input may be driven by TTL or CMOS devices provided that the other input is tied to the

Block Diagram



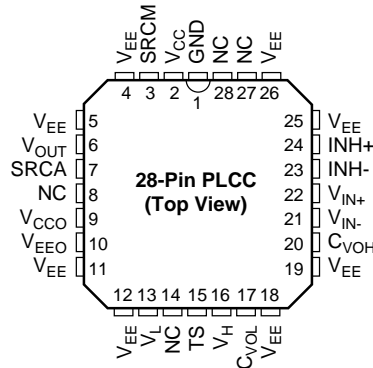
65-5284A

Description (continued)

appropriate threshold value. The pin driver is available in unterminated configuration.

The RC7321 is implemented using Fairchild Semiconductor's high frequency complementary bipolar process.

Pin Assignments



Pin Description

Name	Pin Number	Function
CVOL, CVOH	17	Bypass capacitor for VOH and VOL respectively. Pins CVOL and CVOH should be bypassed to the ground plane with a 1,000 pF chip capacitor placed as close to the pin as possible.
GND	1	Chip ground. Should be connected to the printed circuit board's ground plane at the pin.
INH+ INH-	23, 24	Differential digital inputs. When INH is true (i.e. INH+ > INH-) the driver is forced into the high impedance state. Although these inputs are normally driven by ECL signals, they have a wide enough common mode range that any one of the inputs may be driven by a TTL or CMOS signal provided that the other input is tied to the appropriate threshold voltage.
VCC	2	Quiet positive supply. The nominal value is 10V \pm 3%. For output high voltage levels (VOH) greater than the nominal value of +7V, VCC should be raised 3V above the maximum value of VOH. Whenever VEE is lowered to provide margin at the output low level, VCC should also be lowered by the same amount. VCC should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.
VCCO	9	Positive supply for the RC7321 output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. VCCO should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to VCC.
VEE	4, 5, 11, 12, 18, 19, 25, 26	Quiet negative supply. The nominal value is -5.2V \pm 5%. For output low voltage levels (VOL) less than the nominal value of -2.2V, VEE should be lowered 3V below the minimum value of VOL. Whenever VCC is raised to provide margin at the output high level, VEE should also be raised by the same amount. VEE should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.
VEEO	10	Negative supply for the RC7321 output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. VEEO should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to VEE.

Pin Description (continued)

Name	Pin Number	Function
V _H	16	Analog program input that sets the output high level (V _{OH}). The transfer characteristic from V _H to V _{OH} is nominally unity gain.
V _{IN+} , V _{IN-}	21, 22	Differential digital inputs. The output will toggle between the two levels dictated by V _H and V _L as the differential signal is switched. Although these inputs are normally driven by ECL signals, they have a wide enough common mode range that any one of the inputs may be driven by a TTL or CMOS signal provided that the other input is tied to the appropriate threshold voltage.
V _L	13	Analog program input that sets the output low level (V _{OL}). The transfer characteristic from V _L to V _{OL} is nominally unity gain.
V _O		Driver output on RC7321. The output impedance is 8W ±2Ω. The output is usually back terminated in the characteristic impedance of the transmission line it drives. For a 50Ω line, a 40W±1% resistor should be placed externally as close to the output pin as possible to minimize reflections and ringing. The resistor should also be able to dissipate 0.8W to sustain the short circuit current of the output.
SRCA	7	Slew rate control for both edges. Slew rate of both rising and falling edges decreases as the control current is changed from 0 mA to -0.5 mA. SRC can be programmed with a current DAC or set to a fixed value using a resistor. Increases the speed of the falling edge to match the rising edge.
SRCM	3	
$\overline{\text{TS}}$	15	Active low output notifies thermal shutdown has occurred. In the event of a short circuit or other fault that causes the die temperature to become excessively large, the thermal shutdown will kick in at a die temperature between 125°C and 150°C. If the fault persists, the device will toggle back and forth between shutdown and normal operation at a frequency in the tens of Hertz. $\overline{\text{TS}}$ is an open collector output capable of driving two standard TTL loads. The $\overline{\text{TS}}$ pins of several drivers may be wire-ORed together and input to a latch to indicate an alarm condition.
NC	8, 14, 27, 28	No connection.

Absolute Maximum Ratings¹

Parameter	Min.	Max.	Units
Positive power supply, V _{CC}		13	V
Negative power supply, V _{EE}	-8.2		V
Difference between V _{CC} and V _{EE}		16	V
Input voltage at V _{IN+} , V _{IN-} , IN _{H+} , IN _{H-}	V _{CC} -12	V _{EE} +12	V
Input Voltage at V _H , V _L	V _{CC} -13	V _{EE} +13	V
Differential input voltage, V _{IN+} - V _{IN-} , V _{INH+} - V _{INH-}		6	V
Difference between V _H & V _L (V _H - V _L)		11	V
Input voltage at SRCA	-3	+7	V
Slew rate control current	-2.0		mA
Driver Output Voltage	V _{CC} -13	V _{EE} +13	V
Output voltage at $\overline{\text{TS}}$		5	V
Duration of short-circuit to ground		Indefinite	
Operating temperature range	0	70	°C

Absolute Maximum Ratings¹ (continued)

Parameter	Min.	Max.	Units
Storage temperature range	-65	+125	°C
Lead temperature range (Soldering 10 seconds)		300	°C

Notes:

1. "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameters	Min.	Typ.	Max.	Units
T _C	Case operating temperature		25		°C
V _{CC}	Positive supply voltage	9.7	10.0	10.3	°C
V _{EE}	Negative supply voltage	-5.45	-5.2	-4.95	V
V _{CC-V_{EE}}	Difference between positive and negative supply		15.2	15.8	V
V _{OH} , V _{OL}	Range for output high level and output low level	-2.0		7.0	V
V _{OH-VOL}	Output amplitude	0.1		9.5	V

DC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air) and the load is a 50Ω transmission line with 2.0 ns one-way delay, unless otherwise specified. The transmission line is back-terminated in 50Ω (±5%) using an external resistor.

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
Differential Inputs VIN+, VIN-, VINH+,VINH-						
V _{IN+} , V _{IN-}	Absolute Voltage @ Data Inputs		-2.0		+6.0	V
V _{INH+} , V _{INH-}	Absolute Voltage @ Inhibit Inputs INH+, INH-		-2.0		+6.0	V
V _{ID}	Differential Input Range	V _{IN+} - V _{IN-}	0.4	ECL	5.0	V
V _{DINH}	Differential Inhibit Input Range	V _{INH+} - V _{INH-}	0.4	ECL	5.0	V
I _{IN+} , I _{IN-}	Input Bias Current @ Data Inputs	-2V ≤ V _{IN+} , V _{IN-} ≤ +6V		100	200	μA
I _{INH+} , I _{INH-}	Input Bias Current @ Inhibit Inputs	-2V ≤ V _{INH+} , V _{INH-} ≤ +5V		100	200	μA
Absolute Slew Rate Control Input SRCA						
V _{SRCA}	Compliance Voltage Range		-2.0		+2.0	V
I _{SRCA}	Control Current Range		-0.5		+0.5	V
Matching Slew Rate Control Input SRCM						
V _{SRCM}	Compliance Voltage Range		-2.0		+2.0	V
I _{SRCM}	Control Current Range		-0.5		+0.5	V
Voltage Program Inputs V_H, V_L						
V _H	V _H Range	V _{CC} = 10V; V _{EE} = -5.2V V _{CC} = 12V; V _{EE} = -3.2V V _{CC} = 8V; V _{EE} = -7.2V	-2.0 0 -4.0		+7.0 +9.0 +5.0	V V V
V _L	V _L Range	V _{CC} = 10V; V _{EE} = -5.2V V _{CC} = 12V; V _{EE} = -3.2V V _{CC} = 8V; V _{EE} = -7.2V	-2.5 -0.5 -4.5		+6.0 +8.0 +4.0	V V V

DC Electrical Characteristics (continued)

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
I _H	Bias Current @ V _H	-1V ≤ V _H ≤ +7V; V _L = -2.0V		1.0	2.0	μA
I _L	Bias Current @ V _L	-2V ≤ V _L ≤ +5V; V _H = 6.0V		1.0	2.0	μA
TC _{I_H}	Temperature Drift in I _H	V _H = 7.0V; 25°C ≤ T _C ≤ 70°C output not switching			0.1	μA/°C
TC _{I_L}	Temperature Drift in I _L	V _L = -2.0V; 25°C ≤ T _C ≤ 70°C output not switching			0.1	μA/°C
V _H , LBW	-3 dB bandwidth from V _H or V _L to the output	-1V ≤ V _H ≤ +7V -2V ≤ V _L ≤ +6V; V _H -V _L = 2.0V		50		kHz
Signal Output V_O, V_{OTERM}						
V _O	Output Voltage Range	V _{CC} = 10V; V _{EE} = -5.2V V _{CC} = 12V; V _{EE} = -3.2V V _{CC} = 8V; V _{EE} = -7.2V	-2.2 -0.5 -4.5		+7.0 +9.0 +5.0	V V V
V _A	Amplitude	V _{OH} - V _{OL}	0.3		9.2	V
ΔV _{OH}	Offset to Output High Level	V _H = 0, no load; V _L = -2V ΔV _{OH} = V _H - V _{OH}		±30	±60	mV
ΔV _{OL}	Offset to Output Low Level	V _H = 0, no load; V _H = +7V ΔV _{OL} = V _L - V _{OL}		±30	±60	mV
ΔV _{OH} ΔV _{OL}	Change in V _{OH} output level with change in V _L	V _{OH} = +5V, ΔV _L = 0 to +1V		±10	±15	mV
ΔV _{OL} ΔV _{OH}	Change in V _{OL} output level with change in V _H	V _{OL} = +5V, ΔV _H = +4 to +5V		±10	±15	mV
V _{TC}	Output Voltage Drift	-1V ≤ V _{OH} ≤ +7V; -2V ≤ V _{OL} ≤ +6V;		0.1 0.1		mV/°C
ε _G	Gain Error	-1V ≤ V _{OH} ≤ +7V; -2V ≤ V _{OL} ≤ +6V		1.0 1.0	2.0 2.0	%FS
ε _L	Linearity Error	-2V ≤ V _{OUTPUT} ≤ +7V		0.7	1.0	%FS
Z _{OUT}	Output Impedance (I _{OUT} = 50 mA)		7.0	9.0	11	Ω
I _{ZL}	Output Leakage Current in Inhibit Mode (maintain the following: V _L -1.0V ≤ V _O ≤ V _H +1.0V)	-2.0V ≤ V _O ≤ +7V		0.5	2.0	μA
I _{DC}	DC Current Drive		50			mA
I _{AC}	AC Current Drive		70	100		mA
Thermal Shutdown Output (TS)						
I _{CL}	Short Circuit Current Limit				145	mA
V _{TS}	TS Flag Output Level	I _{OL} = 4 mA			0.5	V
T _{TS}	Shutdown Die Temperature			130	145	°C
Other						
V _{S MAX}	Maximum Rail-to-Rail Supply Voltage	V _{CC} - V _{EE}			16	V
V _{CC}	Positive Supply		+8.0	+10.0	+12.0	V

DC Electrical Characteristics (continued)

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
V _{EE}	Negative Supply		-7.2	-5.2	-3.2	V
I _{CC}	Positive Supply Current			85	90	mA
I _{EE}	Negative Supply Current			90	100	mA
PSR _{VO}	Output Level Power Supply	V _{CC} ; $\Delta V_{CC} = \pm 2.5\%$	40			dB
	Rejection Ratio	V _{EE} ; $\Delta V_{EE} = \pm 2.5\%$	40			dB
PSR _{VSL}	Output Slew Rate Power Supply	V _H = 5V, V _L = 0V, $\Delta V_{CC} = \pm 200$ mV		4.0		%
	Rejection Ratio	V _H = 5V, V _L = 0V, $\Delta V_{CC} = \pm 200$ mV		4.0		%
T _A	Operating Temperature Range	Still Air	0	25	40	°C
		Air Flow > 300 l _{fpm}	0	25	70	°C

AC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air) and the load is a 50Ω transmission line with 2.0 ns one-way delay, unless otherwise specified. The transmission line is back-terminated in 50Ω (±5%) using an external resistor. The measurement probe is a high impedance FET probe with capacitance no greater than 3 pF and resistance no smaller than 10 kΩ.

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
SLR	Slew Rate	V _H - V _L = 5V; Measured between 20% and 80% points. With probe only as load		1.6		V/ns
		With probe and transmission line		1.5		V/ns
t _R , t _F	Rise Time, and Fall Time (Slew rate not adjusted)	Load is Probe Only;				
		V _A = 1V (20% to 80%)		0.6	0.9	ns
		V _A = 3V (10% to 90%)		1.6	2.1	ns
		V _A = 5V (10% to 90%)		2.5	3.0	ns
f	Toggle Rate (Probe only)	Amplitude = 0.8 V _{p-p}	250			MHz
		Amplitude = 5.0 V _{p-p}	125			MHz
t _{PLH}	Low to High Propagation Delay	f = 10 MHz; V _{OH} = +0.4V; V _{OL} = -0.4V		1.6		ns
t _{PHL}	High to Low Propagation Delay	f = 10 MHz; V _{OH} = +0.4V; V _{OL} = -0.4V		1.4		ns
Δt _P	Propagation Delay Match	t _{PLH} - t _{PHL}		200		ps
t _P TC	Propagation Delay Temperature Coefficient			2.0		ps/°C
t _{PWmin}	Minimum Pulse Width	V _H - V _L - 2.0V; pulsewidth at which amplitude drops by 50 mV, measured between 50% points.		2.0		ns
Δt _P PW	Propagation Delay Variation with Pulse Width	2 ns < PW < 98 ns; f = 10 MHz; V _{OH} = +0.4V; V _{OL} = -0.4V		±75		ps
t _{PS}	Preshoot	0.5V < V _A < 5.0V			15mV + 3% of V _A	mV

AC Electrical Characteristics (continued)

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
tOS	Overshoot	$0.5V < V_A < 5.0V$			50mV + 4% of V_A	mV
tS	Output Settling Time	$V_A < 5V$; To within 3% of V_A To within 1% of V_A		8		ns
				10		ns
tPHZ	Propagation Delay from Logic High to Inhibit Mode	$V_{OH} = 1V$; $V_{OL} = -1V$ Load = $100\Omega \parallel 15pF$		2.9		ns
tPLZ	Propagation Delay from Logic Low to Inhibit Mode	Propagation delay is measured to the point at which voltage has changed by 200 mV.		2.9		ns
tPZH	Propagation Delay from Inhibit Mode from Logic High			2.9		ns
tPZL	Propagation Delay from Inhibit Mode to Logic Low			2.9		ns
CZ	Output capacitance in Inhibit Mode			3.0		pF

Notes:

Notes:

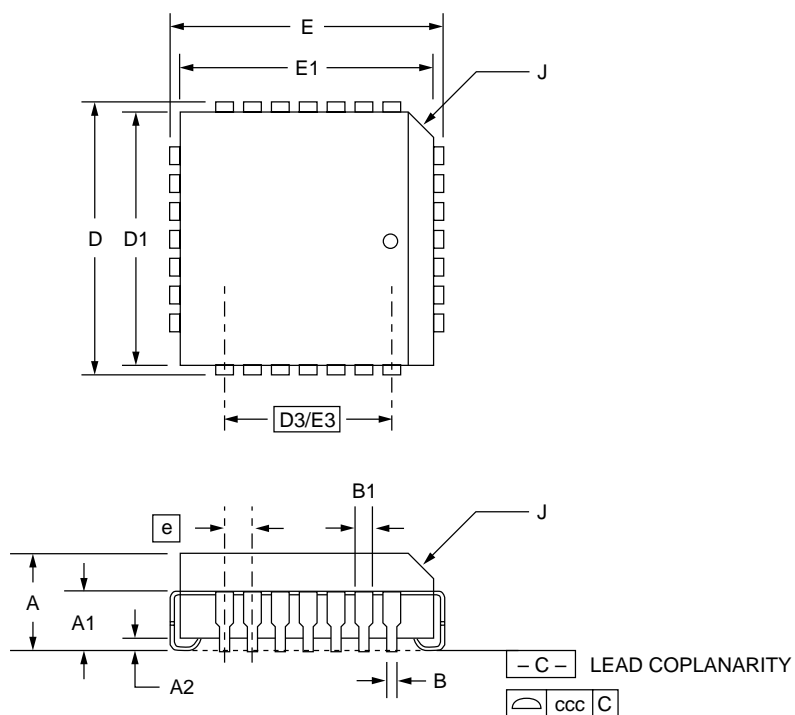
Notes:

Mechanical Dimensions — 28-pin PLCC

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.165	.180	4.19	4.57	
A1	.090	.120	2.29	3.05	
A2	.020	—	.51	—	
B	.013	.021	.33	.53	
B1	.026	.032	.66	.81	
D/E	.485	.495	12.32	12.57	
D1/E1	.450	.456	11.43	11.58	3
D3/E3	.300 BSC		7.62 BSC		
e	.050 BSC		1.27 BSC		
J	.042	.048	1.07	1.22	2
ND/NE	7		7		
N	28		28		
ccc	—	.004	—	0.10	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Corner and edge chamfer (J) = 45°.
3. Dimension D1 and E1 do not include mold protrusion. Allowable protrusion is .101" (.25mm).



Ordering Information

Package	Order Number
28-pin PLCC	RC7321QF

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